



Mono BTL Audio Power Amplifier

Application Note

Demonstration Board - AUD4990/AUD4991

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1. Overview and Scope

This application note is intended to describe the Mono BTL Audio Power Amplifier (AUD4990, AUD4991) and related circuitry within its demonstration board. This document includes the schematic, PCB layout and application highlights.

2. General Description

The AUD4990 is a high power and low noise distortion Mono BTL Audio Power Amplifier. It is suitable for mono or stereo applications with single-ended mode. The AUD4990/AUD4991 amplifier can drive 8ohm speaker load with THD+N < 1% and output power up to 1W. The output gain can be controlled by changing the feedback resistor R1, R2, R3 and R4 (refer to Figure 1 for details). For power saving, AUD4990/AUD4991 also provides the shutdown mode by SD mode and SD pins.

3. Feature

Product	Description	Supply Voltage (V)	Vos (mV) Limit	PSRR (dB)	Ton (ms)	IQ (mA)	Package
AUD4990	2W Audio Power Amplifier with Selectable Shutdown	2.7 to 5.5	25	68	100	2.5	DFN-10 MSOP-8
AUD4991	High Performance 2W Audio Power Amplifier with Selectable Shutdown	2.7 to 5.5	10	68	100	2.5	DFN-10

4. AUD4990 / AUD4991 Application – Demonstration Board

AUD4990/AUD4991 can use the same demonstration board with MSOP-8 or DFN-10 package. The demonstration board schematic is shown on Figure 1. The demo board contains two AUD4990/AUD4991 with MSOP-8 and DFN-10 packaging. AUD4990/AUD4991 is configured for single-ended audio amplifier with gain = 2, where R1, R2, R3 and R4 = 20Kohm. The shutdown mode can be controlled by J8, J5 and J9 (see Table 1 for more details).

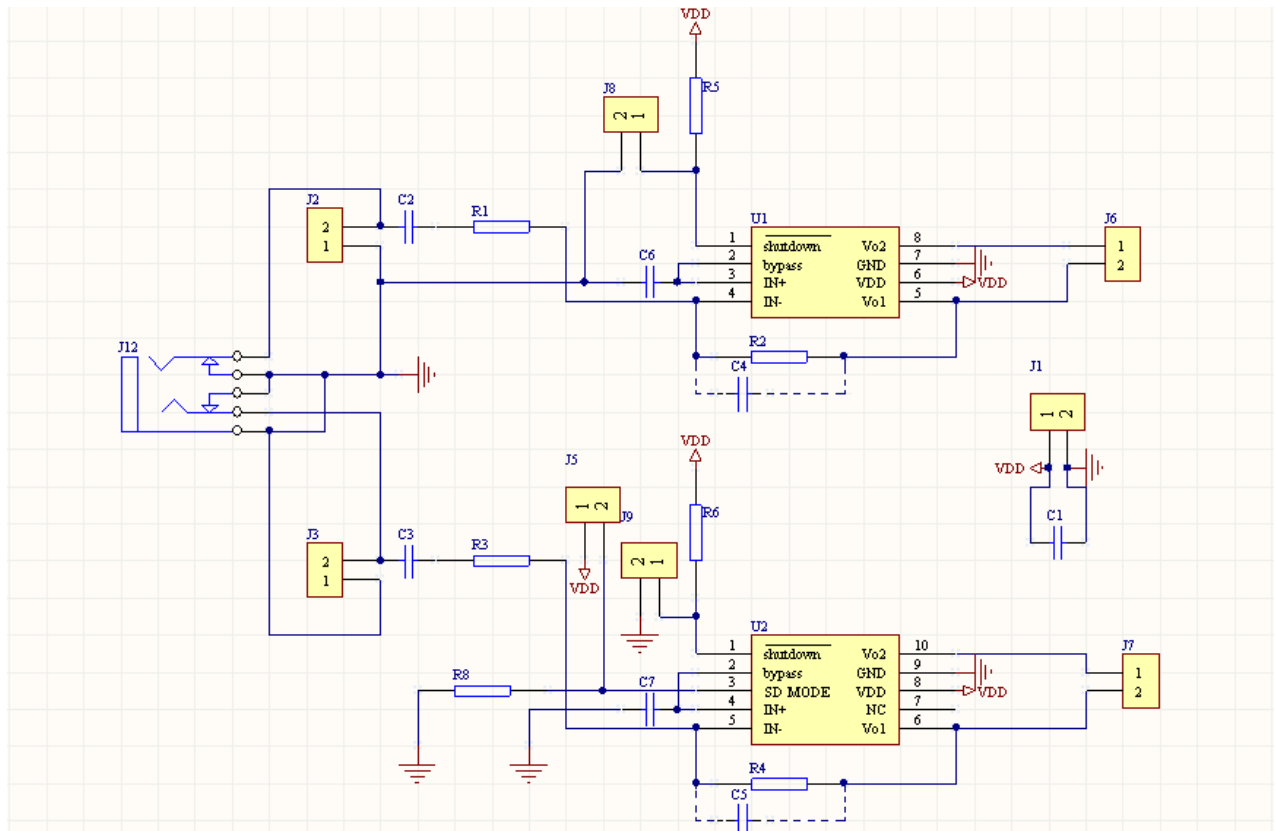


Figure 1 – Demonstration Board Schematic

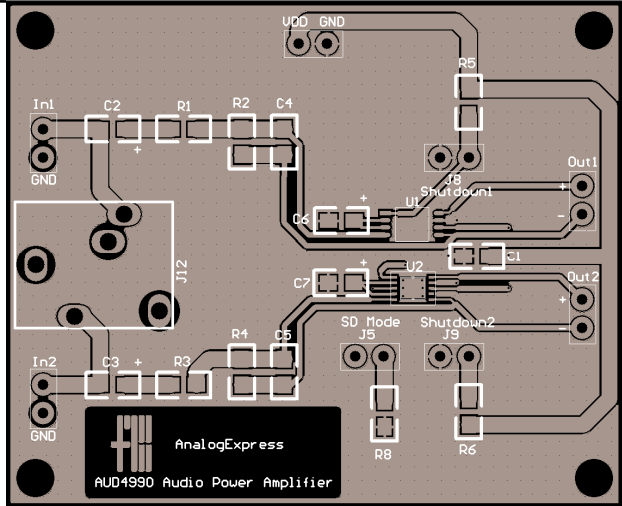


Figure 2 – PCB Layout (Top View)

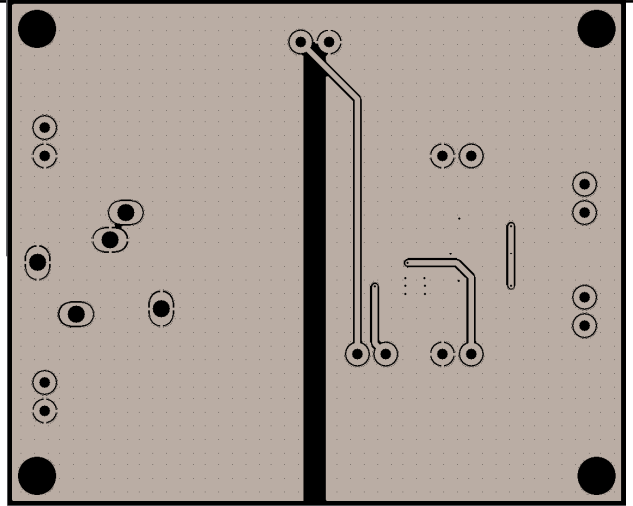


Figure 3 – PCB Layout (Bottom View)

J8 (U1 – Shutdown)	J5 (U2 – SD Mode)	J9 (U2 – Shutdown)	U1 - Status	U2 - Status
Short	X	X	Shutdown	X
Open	X	X	On	X
X	Open	Short	X	Shutdown
X	Open	Open	X	On
X	Short	Short	X	On
X	Short	Open	X	Shutdown

* SD mode and SD pins cannot be left floating, they must be connected to V_{DD} or V_{SS}

Table 1 – Shutdown Mode Configuration

5. Components Description

Part #	Description
U1	AUD4990MS08
U2	AUD4990D10-3 / AUD4991D10-3
VDD(J1)	AUD4990/AUD4991 Power supply input (2.7V~5.5V)
VDD(J1)	AUD4990 / AUD4991 Power supply input (2.7V~5.5V)
GND(J1)	AUD4990 / AUD4991 Ground
In1(J2), In2(J3)	AUD4990 / AUD4991 IN1- negative differential input
Out1(J6), Out2(J7)	AUD4990 / AUD4991 BTL output
C1	Power supply bypass capacitor for filtering (Note 1)
C2, C3	Input coupling capacitor of AUD4990 / AUD4991 at input terminals. It can block the input signal's DC voltage. It also acts as a high-pass filter with inverting input resistance (R_1, R_3). The cutoff frequency is (f_c) = $1 / 2\pi * R_1 * C_2$ for U1 and $f_c = 1 / 2\pi * R_3 * C_3$ for U2
C4, C5	Bypass capacitor for reducing the noise (optional)
C6, C7	Bypass capacitor for half-supply filtering (Note 1)
R1, R3	Input resistor to the inverting differential input which sets the closed-loop gain in conjunction with R2/R4
R2, R4	Feedback resistor of audio amplifier to set the closed-loop gain in conjunction with R1/R2
R5, R6	Pull up resistor which provides the logic high level to Shutdown1 and Shutdown2 pin
R8	Pull up resistor which provides the logic high level to SD mode pin of U2
J5	To control the SD mode of U2 (AUD4990 / AUD4991). Refer to Table 1 for detail setup
J8, J9	To enable / exit shutdown feature (refer to Table 1 for detail setup)
J12	Stereo phone jack socket

Note:

1. Power supply/half supply bypass capacitor is used for filtering power supply noise to maximize the power supply rejection and reduce the noise. The bypass capacitor should be placed as close to the device's power supply pins on the PCB layout. Selection of power supply capacitor will affect the PSRR requirement, click and power performance and the cost. A large input capacitor isn't cost effective and wastes the PCB area. In typical applications, bypass power supply capacitor with 1 μ F is recommended to optimize the click and pop performance.

6. Power Up Procedure

- i) Set AUD4990 in shutdown mode (SD mode = GND and SD = 0 or SD mode = VDD and SD = 1)
- ii) Apply V_{DD} voltage to AUD4990 ($V_{DD} = 2.7V \sim 5.5V$)
- iii) Input the signal to Vin pin
- iv) Exit the shutdown mode by setting SD = 1, if SD mode = GND or SD = 0, if SD mode = 0

7. Application Highlight

1. All logic inputs to the IC must be low or high and cannot be left floating.
2. IN input range is related to the V_{DD} voltage supply. If the IN input is too high the output will be cropped with a poor THD+N reading.
3. Audio amplifier gain can be controlled by the feedback resistor R1, R2, R3 and R4. Higher gain will provide the higher output with the same signal input. However the THD+N will be also degraded, as the noise will be amplified at the same time.
4. Stereo phone jack (J12) signal input is connected to ground when not connected to the stereo phone plug. When In1 / In2 is used as the input terminal, the stereo phone plug needs to be connected to the stereo phone jack, otherwise the In1 / In2 pins are shorted to ground.

5. Output Gain

AUD4990 / AUD4991 gain is controlled by the resistor ratio of R1 and R2, and R3 and R4. The equation is shown on eq1:

$$A_v = 2 * \frac{R_2}{R_1} \text{ for U1 and } A_v = 2 * \frac{R_4}{R_3} \text{ for U2(eq1)}$$

6. Power Dissipation

Power dissipation is a major concern item for designing an amplifier. The power dissipation of AUD4992 (per channel) is four times of a single-ended amplifier. The power dissipation equation is derived from eq2:

$$P_{DT} = \frac{1}{R_L} \left(\frac{8}{\pi} \sqrt{\frac{P_{OUT} R_L}{2} \frac{V_{DD}}{2}} - P_{OUT} R_L \right) \text{(eq2)}$$

where:

P_{DT} denotes the power dissipation for the BTL amplifier

P_{OUT} denotes the power output

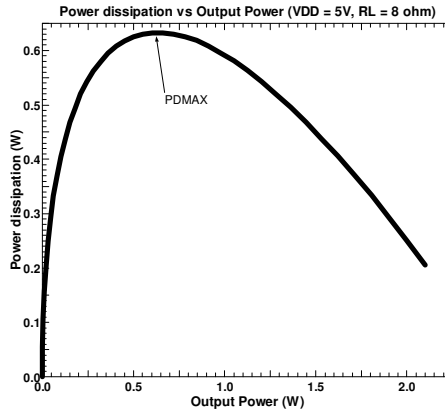
R_L is the resistance of the load

V_{DD} denotes the supply voltage

7. Maximum Power Dissipation

Maximum power dissipation is deviated from eq2. It is a critical parameter to prevent thermal Shutdown in normal applications:

$$P_{D_{MAX}} = \frac{4 * V_{DD}^2}{2\pi^2 R_L} \dots\dots\dots(eq3)$$



8. Thermal Background

To prevent thermal shutdown (TSD) on the normal application, the max power dissipation and IC's junction-to-case thermal resistance must be considered for designing an amplifier.

The maximum power dissipation should not case the IC thermal shutdown and it can be found in eq4:

$$P_{D_{MAX}} = (T_{J_{MAX}} - T_A) / \theta_{JA} \dots\dots\dots(eq4)$$

where:

P_{D_{MAX}} denotes the maximum power dissipation

T_{J_{MAX}} denotes the maximum junction temperature

T_A denotes the ambient temperature

θ_{JA} denotes the junction-to-case thermal resistance

8. Application Example

Figure 4 – Block Diagram for Smart Phone System

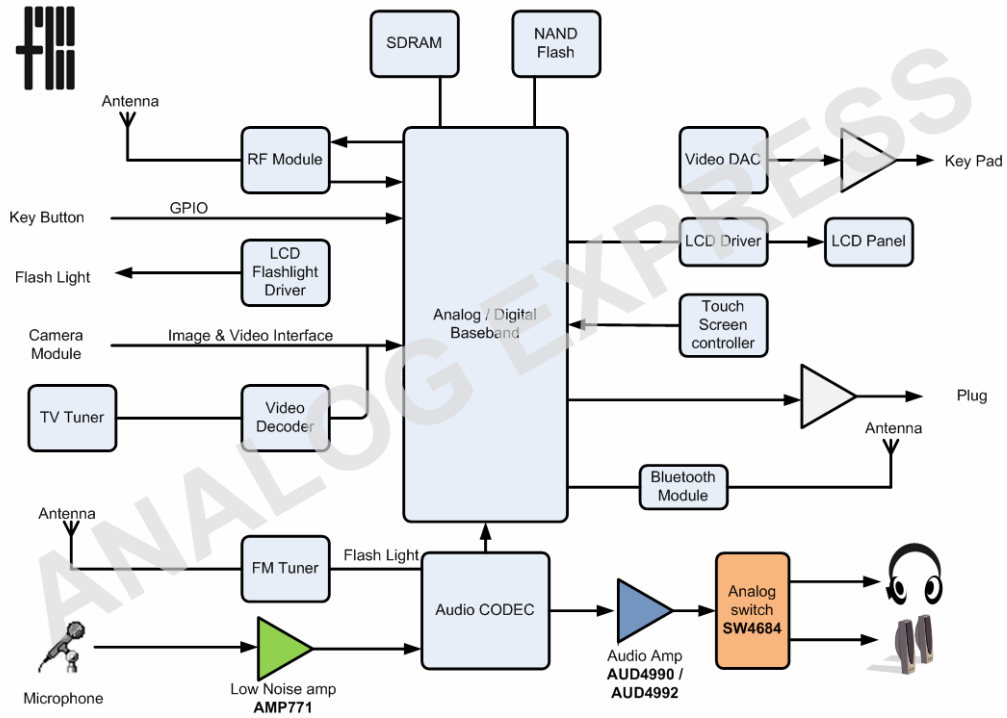
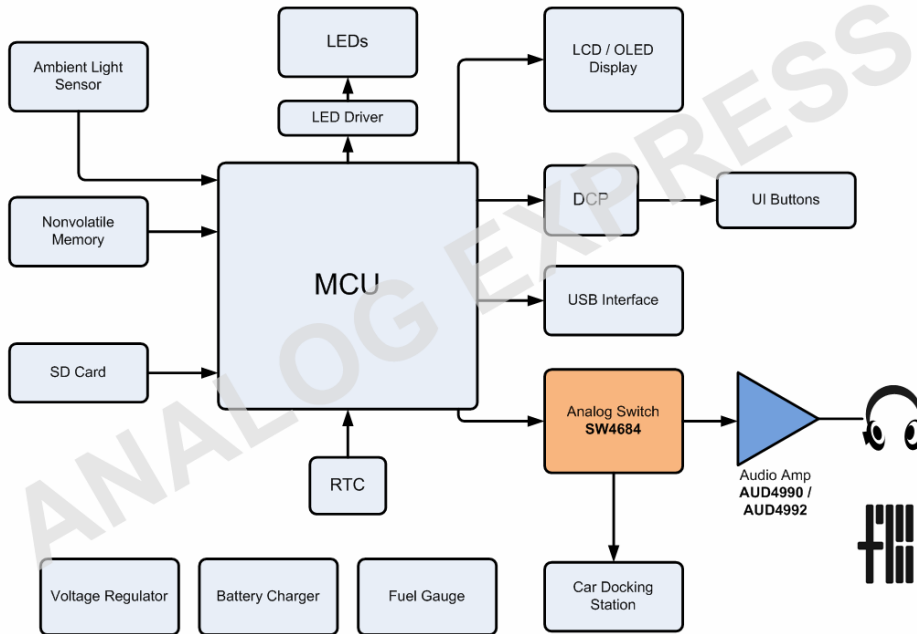


Figure 5 – Block Diagram for MP3 System



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Analog Express Inc.

US Tel: (1) 713 666 9459

HK Tel: (852) 2527 5009

www.analogexpress.com

Email: sales@analogexpress.com

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1.1	7-Jan-08	Proven update	Louis Cheung	