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Fully Differential Audio Power Amplifier

Application Note

Demonstration Board- AUD5006

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1. Overview and Scope

This application note is intended to describe the Fully Differential Audio Power Amplifier (AUD5006) and related circuitry within its demonstration board. This document includes the schematic, PCB layout, power up procedure and application highlight

2. General Description

AUD5006 is a high power and low noise, low distortion fully differential audio power amplifier. It is suitable for differential input audio application. AUD5006 amplifier can drive 8 ohm speakers load with THD+N < 1% and delivers output power up to 1W or drive 4 ohm speakers load with output power up to 2W with high PSRR. The output gain can be controlled by changing the feedback resistor R1, R2, R3 & R4 (refer to Figure 1 for detail) or using built-in resistor network. For power saving, AUD5006 also provides shutdown mode by SD pin.

3. Feature

Product	Description	Supply Voltage	Vos (mV)	PSRR (dB)	x-talk (dB)	Ton (ms)	IQ (mA)	Package
AUD5006	2 + 2W Stereo Fully Differential Audio Power Amplifier	2.7 to 5.5	30	70	100	10	4.5	DFN-14

4. AUD5006 Application – Demonstration Board

AUD5006 demonstration board use AUD5006 DFN14 package with fully differential audio amplifier application. The demonstration board schematic is shown in Figure 1, PCB layout is shown in Figure 2 to Figure 5. AUD5006 has a gain control pin to configure the gain AV = 12dB / 15.6dB / 18dB. The gain is adjusted by input resistor R1, R2, R3 and R4 when G1&G0 = 1. The shutdown mode and mute mode can be controlled by shutdown and mute pins respectively.(see Table 1 for more detail).

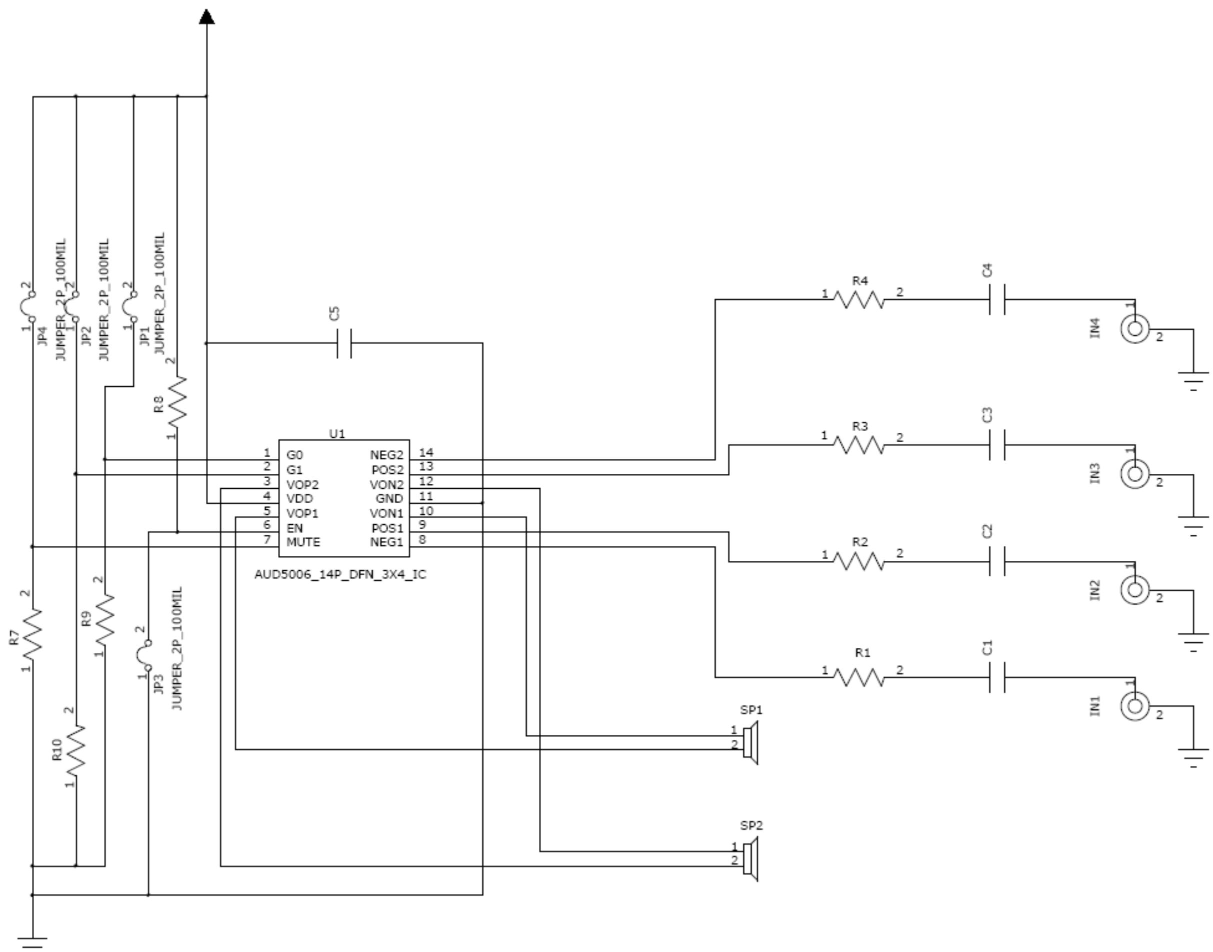


Figure 1 – Demonstration Board Schematic

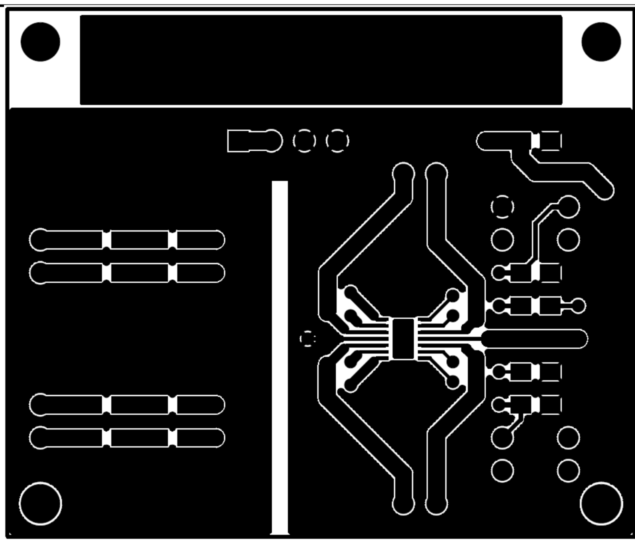


Figure 2 – PCB Layout (Top View)

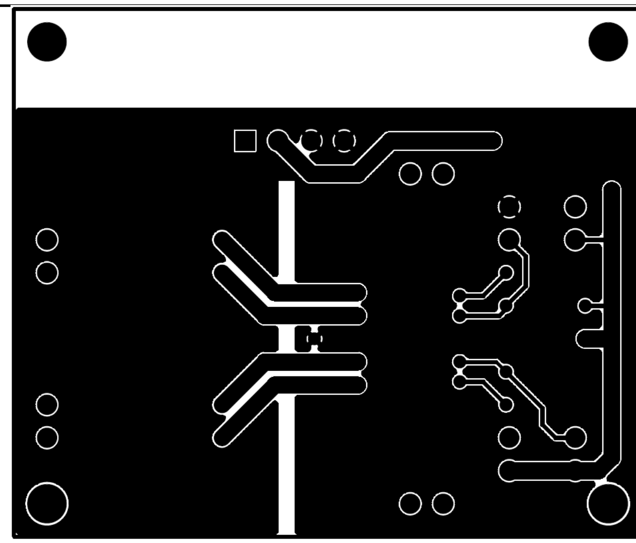


Figure 3 – PCB Layout (Bottom View)

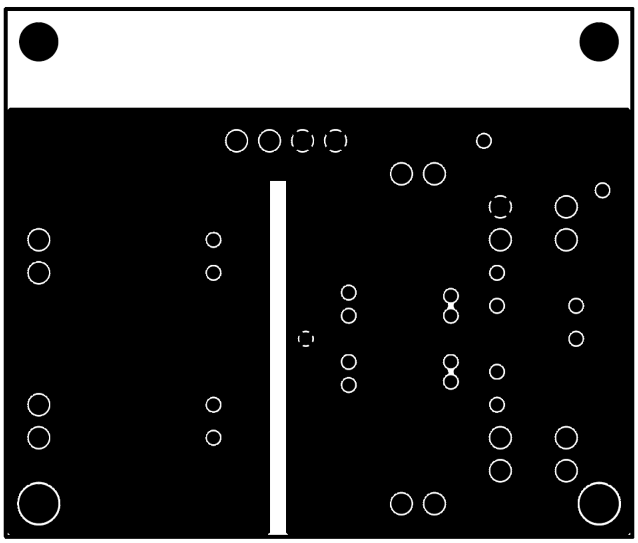


Figure 4 – PCB Layout (Inner1/2 View)

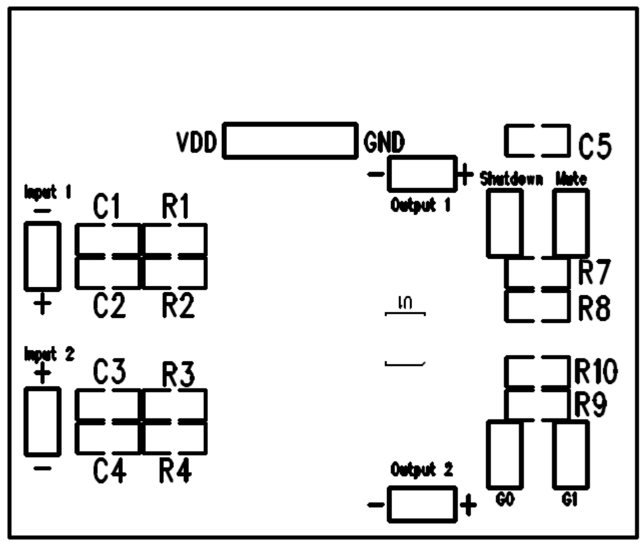


Figure 5 – Silkscreen

G1	G0	Gain
Open	Open	12dB
Open	Short	15.6dB
Short	Open	18dB
Short	Short	External

Table 1 – Gain mode configuration

Shutdown	Status
Open	Normal Mode
Short	Shutdown Mode

Table 2 – Shutdown mode configuration

Mute	Status
Open	Normal Mode
Short	Mute Mode

Table 3 – Mute mode configuration

* All logic input pins cannot be left floating, they must be connected to V_{DD} or V_{SS}

5. Components Description

Part #	Description
U1	AUD5006D14-4
VDD	AUD5006 power supply Input (2.7V~5.5V)
GND	AUD5006 ground
Input 1 + / -	AUD5006 IN1+ and IN1- differential input of channel 1
Input 2 + / -	AUD5006 IN2+ and IN2- differential input of channel 2
Output 1 + / -	AUD5006 VO1+ and VO1- differential output of channel 1
Output 2 + / -	AUD5006 VO2+ and VO2- differential output of channel 2
Shutdown	To enable / exit shutdown feature (refer to Table 2 for detail setup)
Mute	To enable / exit mute feature (refer to Table 3 for detail setup)
C1~C4	Input coupling capacitors of AUD5006 at input terminals. It can block the DC voltage of input signal. It also acts as a high-pass filter with inverting input resistance (R_1, R_2, R_3, R_4). The cutoff frequency (f_C) = 1 / (2π * $R_{1/2}$ * $C_{1/2}$) for CH1 and f_C = 1 / (2π * $R_{3/4}$ * $C_{3/4}$) for CH2 of external mode (G0 & G1 = 1). R_i is equal to 15K for internal gain mode.
C5	Power supply bypass capacitor for filtering (Note 1)
R1~R4	Input resistors to the differential input which set the closed-loop gain in conjunction with internal feedback resistor (~60k ohm) of CH1 and CH2
R7, R9, R10	Pull down resistors which provide logic low level to G0, G1 & mute pins.
R8	Pull up resistor which provide logic high level to shutdown pin.

Note:

1. Power supply bypass capacitor is used for filtering power supply noise to maximize the power supply rejection and reduce noise. The bypass capacitor should be placed as close to the device's power supply pins on the PCB layout as possible. Selection of power supply capacitor will affect PSRR performance, click and pop performance and cost. Large input capacitor isn't cost effective and wastes PCB area. In typical application, bypass power supply capacitor of 1uF is recommended to optimize the click and pop performance.

6. Power Up Procedure

i) Set AUD5006 in shutdown mode (shutdown = V_{SS} / Short)

ii) Apply V_{DD} voltage to AUD5006 (V_{DD} = 2.7V ~ 5.5V)

iii) Input the signal to Input 1 and Input 2

iv) Exit the shutdown mode by setting shutdown = V_{DD} / Open

7. Application Highlight

1. All Logic inputs to the IC must be low or high and cannot be left floating.
2. Differential input range must be less than the supply voltage V_{DD}. If the differential input is too high the output will be cropped with poor THD+N reading and distortion.
3. Audio amplifier gain can be controlled by the input resistor R1, R2, R3 and R4. Higher gain provides the higher output with the same signal input. However THD+N will be also degraded as noise will be amplified at the same time.
4. Output Gain

   Gain of AUD5006 is controlled by the resistor ratio of R1 & R2 and R3 & R4 at external gain mode. The equation is shown as eq1

$$A_V = \frac{R_f}{R_i}, where\ R_f = 60k\Omega\ \ for\ \ external\ \ gain\ \ \mathrm{mod}\, e,$$

$$R_i = R_1, R_2, R_3, R_4\ \ \&\ \ R_1 = R_2; R_3 = R_4\ ....(eq1)$$

5. Power Dissipation

   Power dissipation is major concern for designing an amplifier. The power dissipation of AUD5006 (per channel) is four times that of a single-ended amplifier. The power dissipation equation is derived at eq2

$$P_{DT} = \frac{1}{R_L}\left(\frac{8}{\pi}\sqrt{\frac{P_{OUT}R_L}{2}}\frac{V_{DD}}{2} - P_{OUT}R_L\right)..(eq2)$$

   where

   P_{DT} denotes the power dissipation for BTL amplifier,

   P_{OUT} denotes the power output,

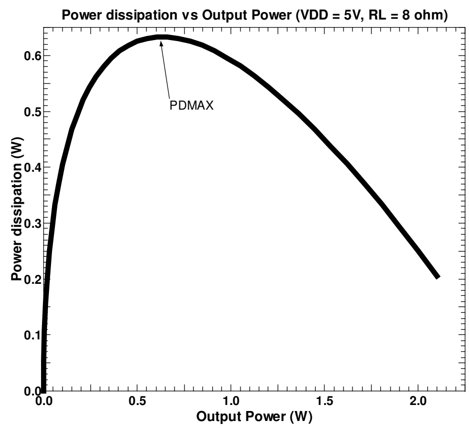
   R_L is the resistance of the load,

   V_{DD} denotes the supply voltage

7. Maximum Power Dissipation

Maximum power dissipation is derived at eq3. It is a critical parameter to prevent the thermal shutdown under normal application.

$$P_{DMAX} = \frac{4 * V_{DD}^{\ 2}}{2\pi^2 R_L} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(eq3)$$



8. Thermal Shutdown

To prevent thermal shutdown (TSD) under normal application, the max power dissipation and IC's junction-to-case thermal resistance must be consider when designing an amplifier.

The maximum power dissipation should not exceed the IC thermal shutdown and it can be found form (eq4)

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(eq4)$$

where

P_{DMAX} denotes the maximum power dissipation

T_{JMAX} denotes the maximum junction temperature

T_A denotes the ambient temperature

θ_{JA} denotes the junction-to-case thermal resistance

8. Application Example

Figure 6 – Block Diagram for Smart Phone System

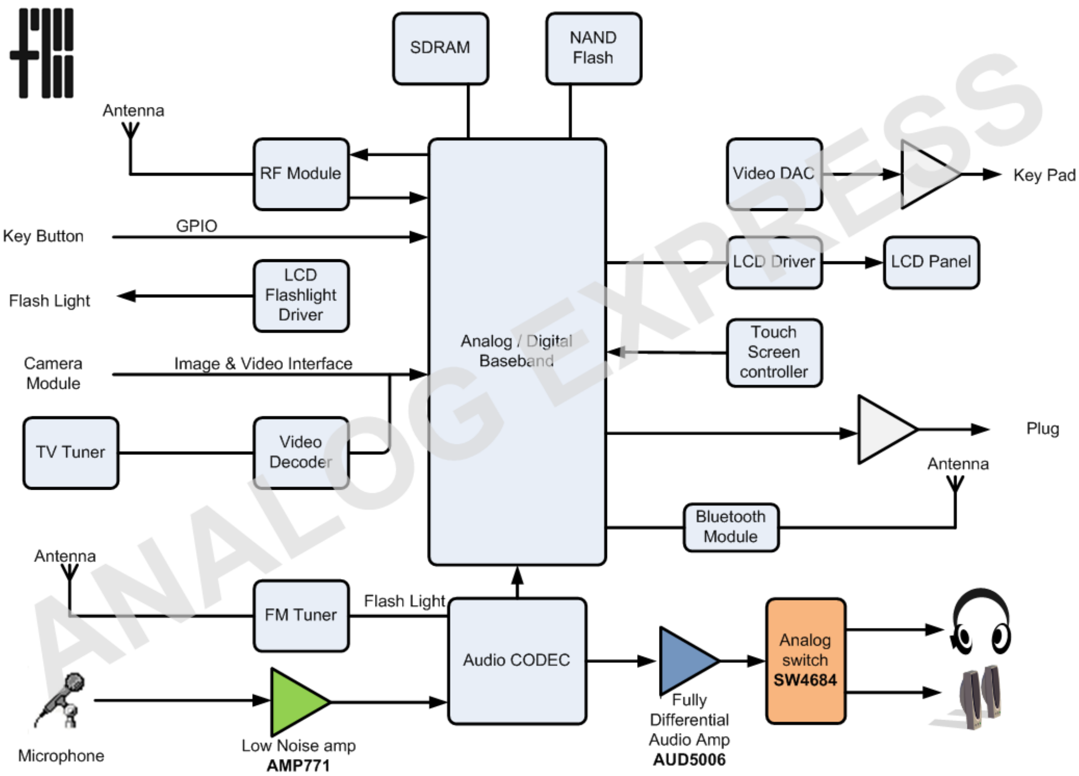
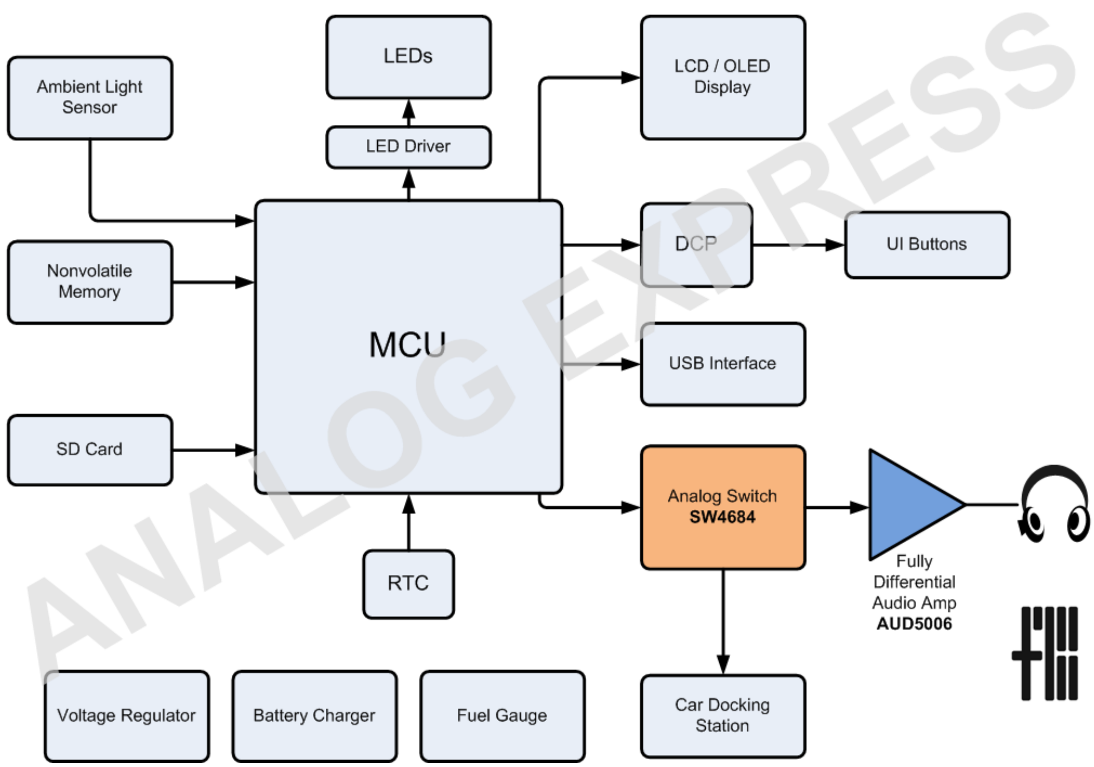


Figure 7 – Block Diagram for MP3 System



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